

1

2

3

4

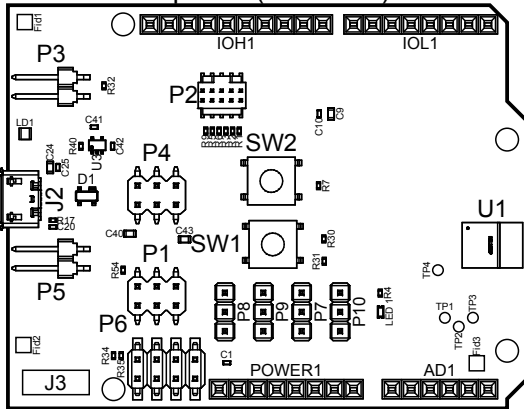
1

2

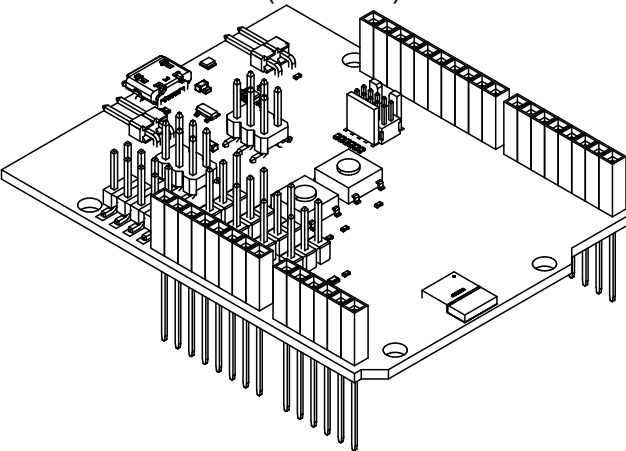
3

4

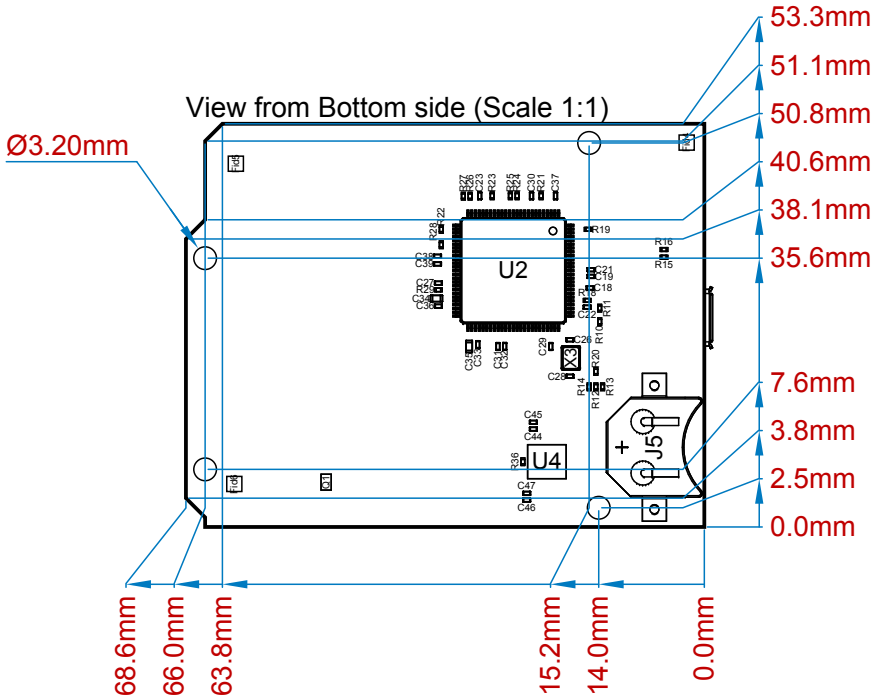
View from Top side (Scale 1:1)



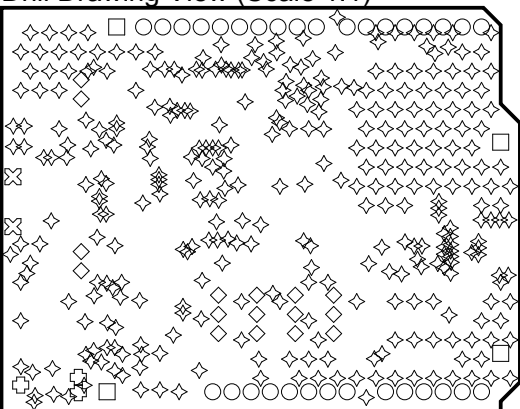
View from Front side (Scale 1:1)



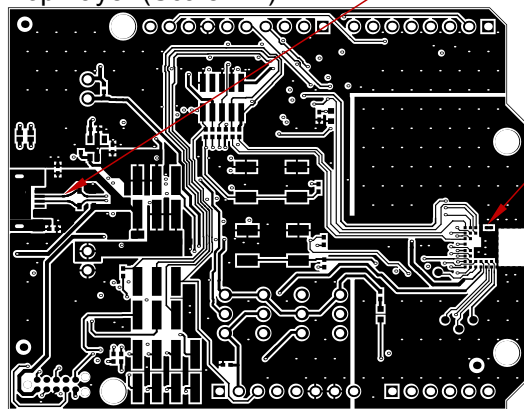
View from Bottom side (Scale 1:1)



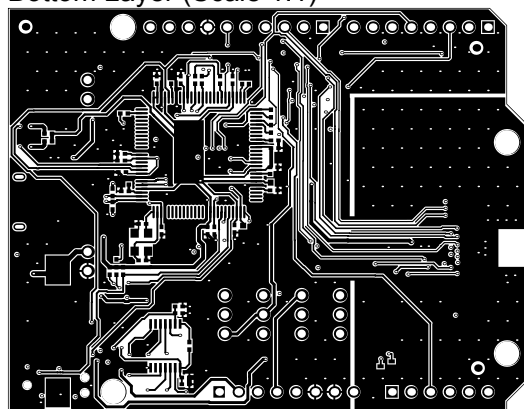
Drill Drawing View (Scale 1:1)



Top Layer (Scale 1:1)



Bottom Layer (Scale 1:1)



Drill Table

| Symbol | Count | Hole Size | Plated | Hole Type | Drill Layer Pair | Via / Pad |
|-----------|-------|-----------|------------|-----------|--------------------------|-----------|
| ◇ | 343 | 0.20mm | Plated | Round | Top Layer - Bottom Layer | Via |
| ⊗ | 2 | 0.50mm | Plated | Slot | Top Layer - Bottom Layer | Pad |
| ⊙ | 3 | 0.99mm | Non-Plated | Round | Top Layer - Bottom Layer | Pad |
| ○ | 32 | 1.02mm | Plated | Round | Top Layer - Bottom Layer | Pad |
| ◇ | 16 | 1.10mm | Plated | Round | Top Layer - Bottom Layer | Pad |
| □ | 4 | 3.20mm | Non-Plated | Round | Top Layer - Bottom Layer | Pad |
| 400 Total | | | | | | |

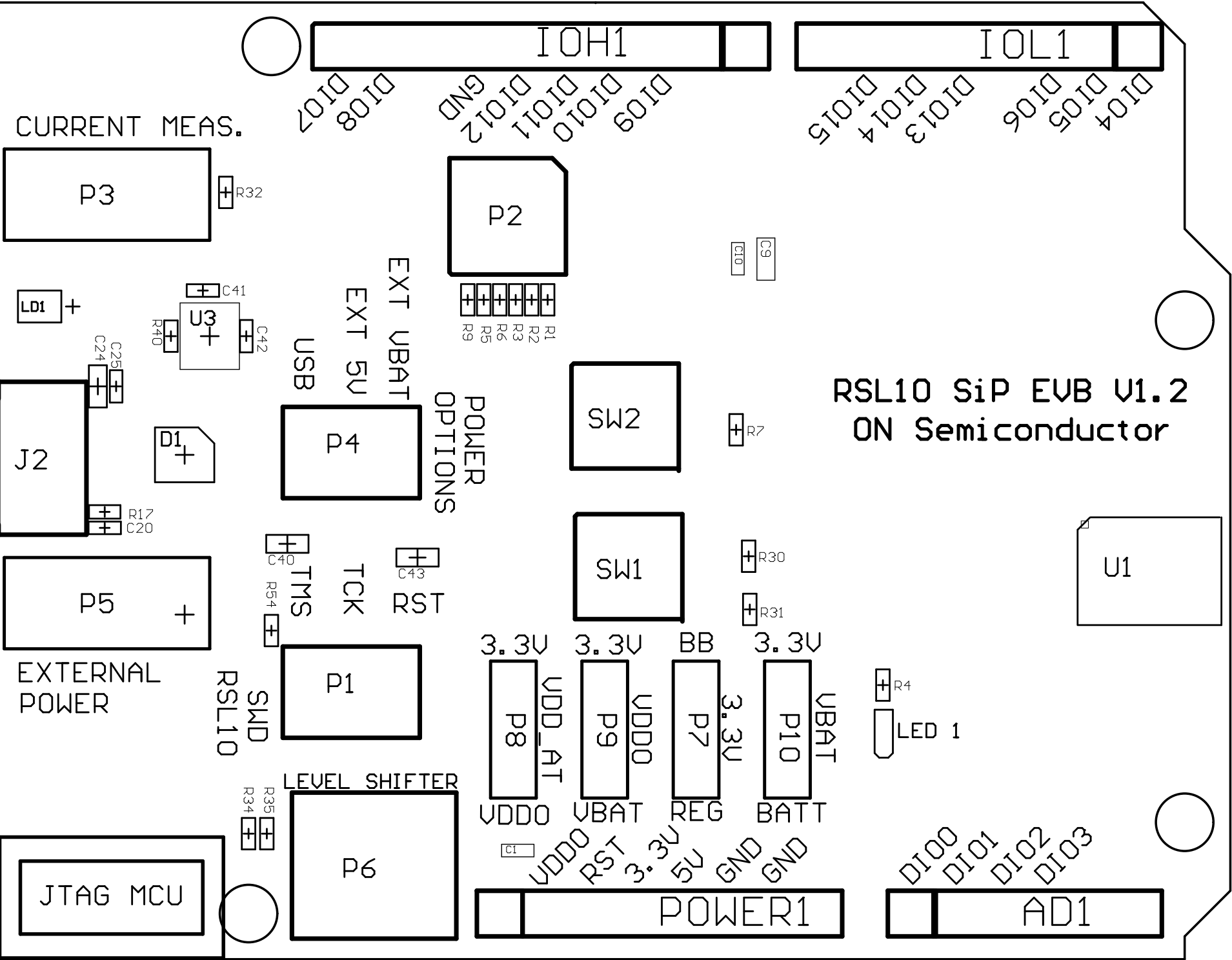
Layer Stack Legend

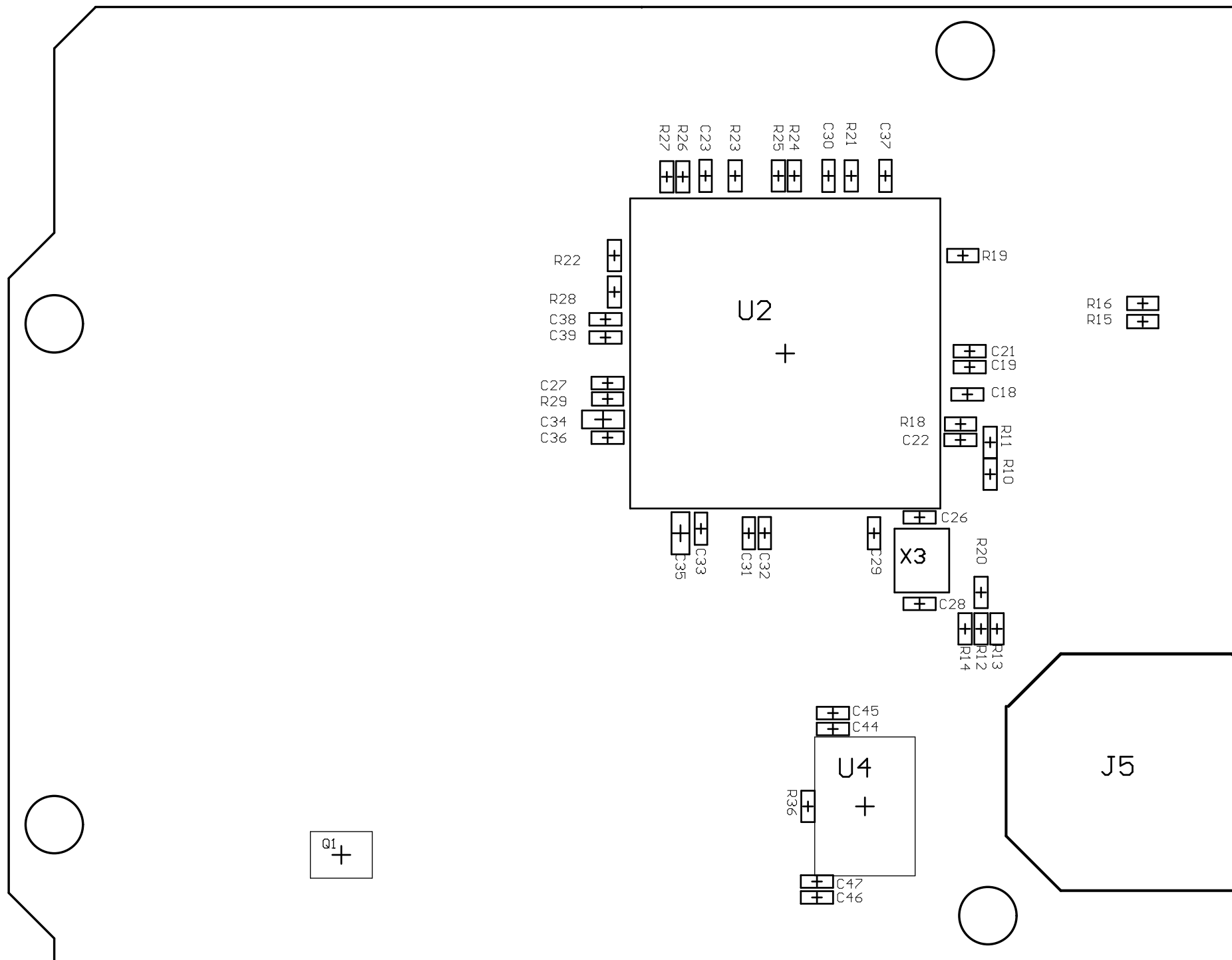
| Material | Layer | Thickness | Dielectric Material | Type | Gerber |
|--------------------------------|----------------|---------------|---------------------|-------------|--------|
| | Top Paste | | | Paste Mask | GTP |
| | Top Overlay | | | Legend | GTO |
| Surface Material | Top Solder | 0.01mm(0mil) | Solder Resist | Solder Mask | GTS |
| Copper | Top Layer | 0.05mm(2mil) | | Signal | GTL |
| Prepreg | | 0.23mm(9mil) | FR-4-370HR | Dielectric | |
| Copper | Signal Layer 1 | 0.02mm(1mil) | | Signal | G1 |
| Core | | 0.91mm(36mil) | FR4-370HR | Dielectric | |
| Copper | Signal Layer 2 | 0.02mm(1mil) | | Signal | G2 |
| Prepreg | | 0.23mm(9mil) | FR-4-370HR | Dielectric | |
| Copper | Bottom Layer | 0.05mm(2mil) | | Signal | GBL |
| Surface Material | Bottom Solder | 0.01mm(0mil) | Solder Resist | Solder Mask | GBS |
| | Bottom Overlay | | | Legend | GBO |
| | Bottom Paste | | | Paste Mask | GBP |
| Total thickness: 1.53mm(60mil) | | | | | |

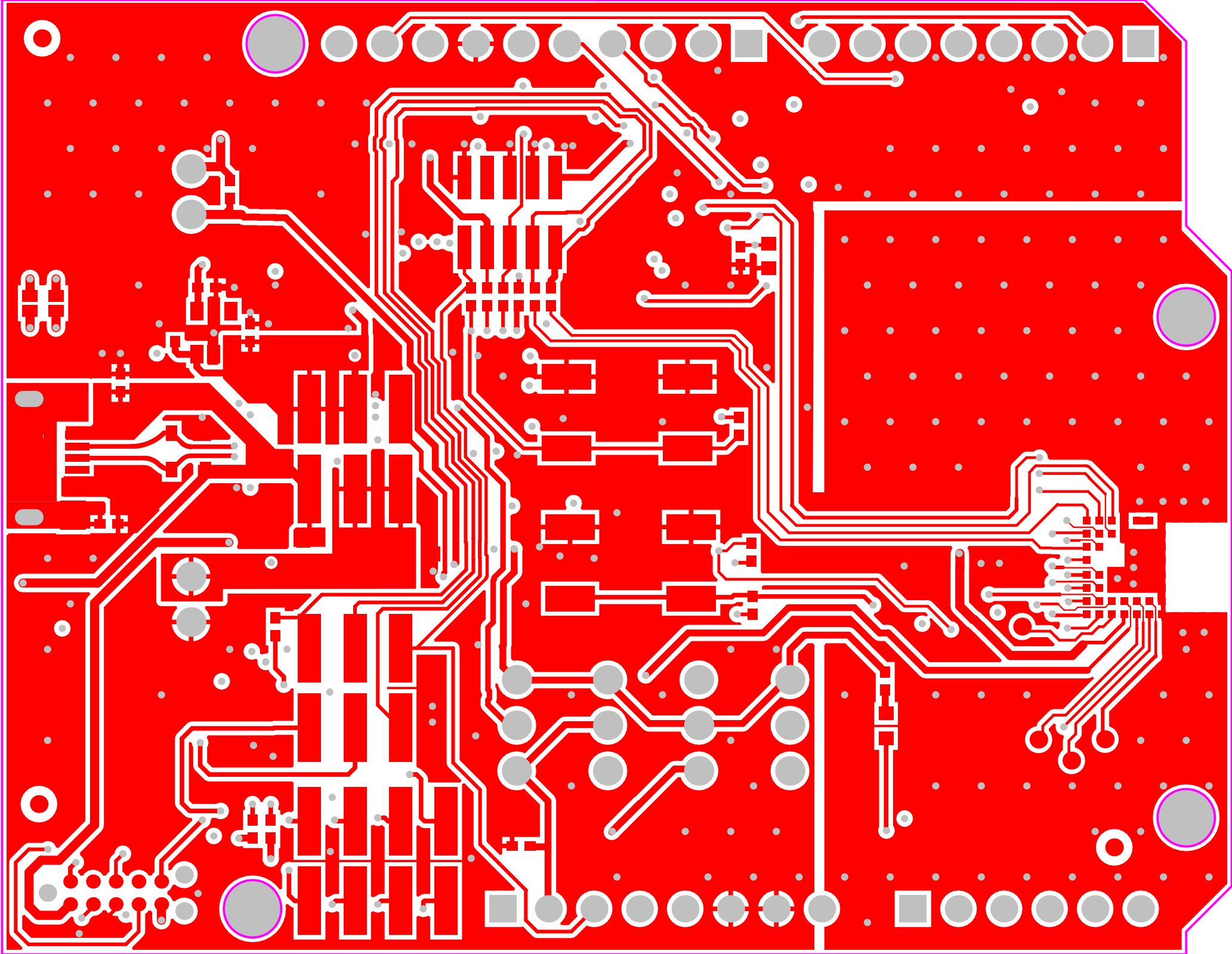
1. Fabricate to IPC6012 Class2.
2. Board material, Isola 370HR RoHS Compliant with nominal thickness of 0.062 INCH, 1/2 OZ copper on top and bottom layers, 1/2 OZ copper on inner layers.
3. Order of layers is Top_Layer, Signal_Layer1, Signal_Layer2, Bottom_Layer.
4. All dimensions +/- 5 MIL, unless otherwise specified.
5. LDI mask both sides, mask must be between lands. Minimum of 1.5 MIL per side around lands.
6. Silkscreen to be white ink, soldermask green. No ink to be on surface mount land pads. Vendor marking on bottom side.
7. Board to use ENIG (Electroless Nickel Immersion Gold) finish.
8. Board to be 100% tested to Gerber net list file.
9. Include a minimum of two fiducias per panel.
10. Controlled impedance board: Top_Layer -microstrip,Signal_Layer1-gnd.RF_50ohm microstrip (0.4mm) traces on top layer shall be 50 ohms +/-10%.
11. USB Diff pair controlled impedance to be 90 ohm +/-10%, DHSD_N and DHSD_P traces.
12. Minimum copper hole wall plating 1 MIL.
13. Maximum warp/twist 0.005 INCH per INCH.
14. Finish all conductors +0.000/-0.002 INCH from supplied artwork.

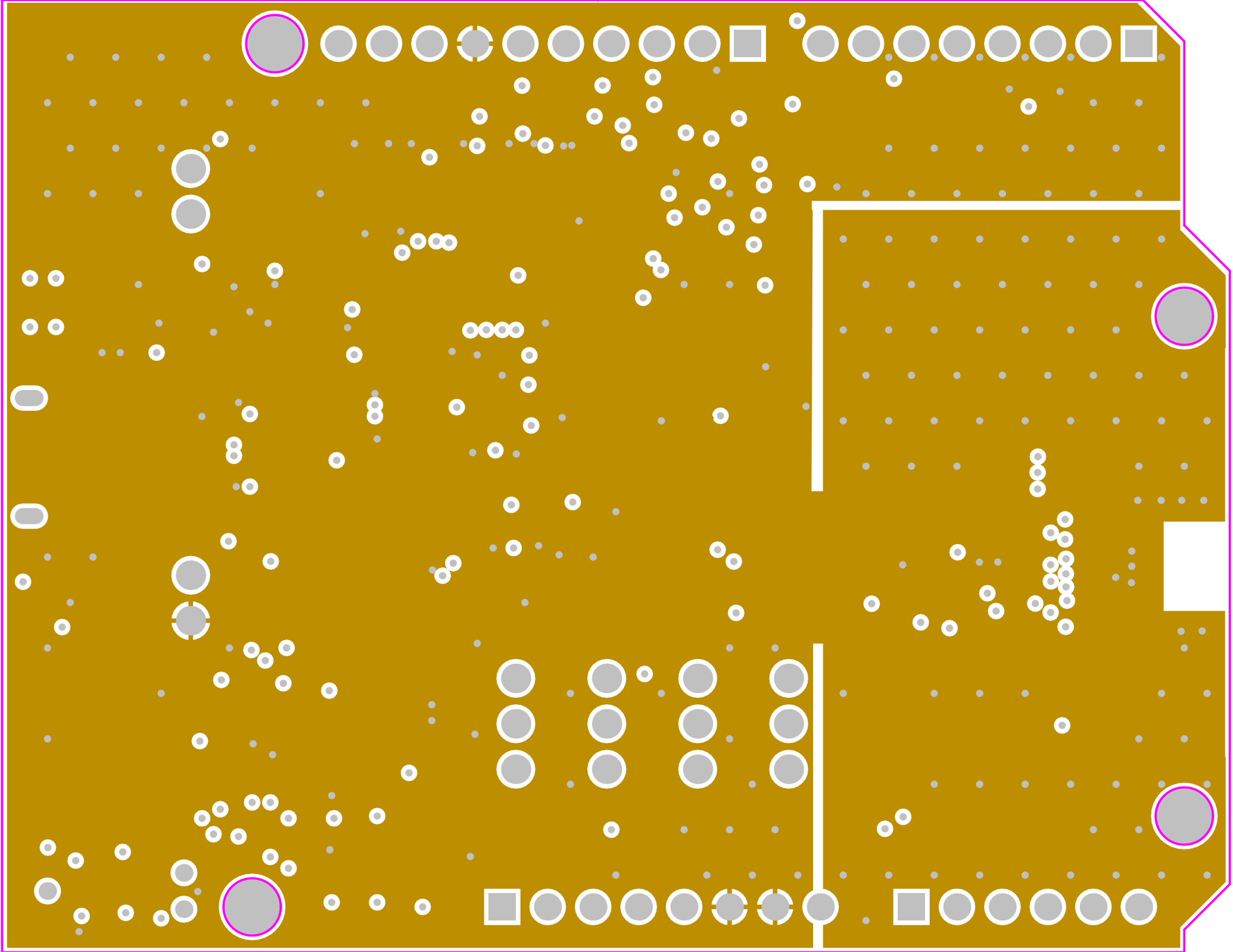
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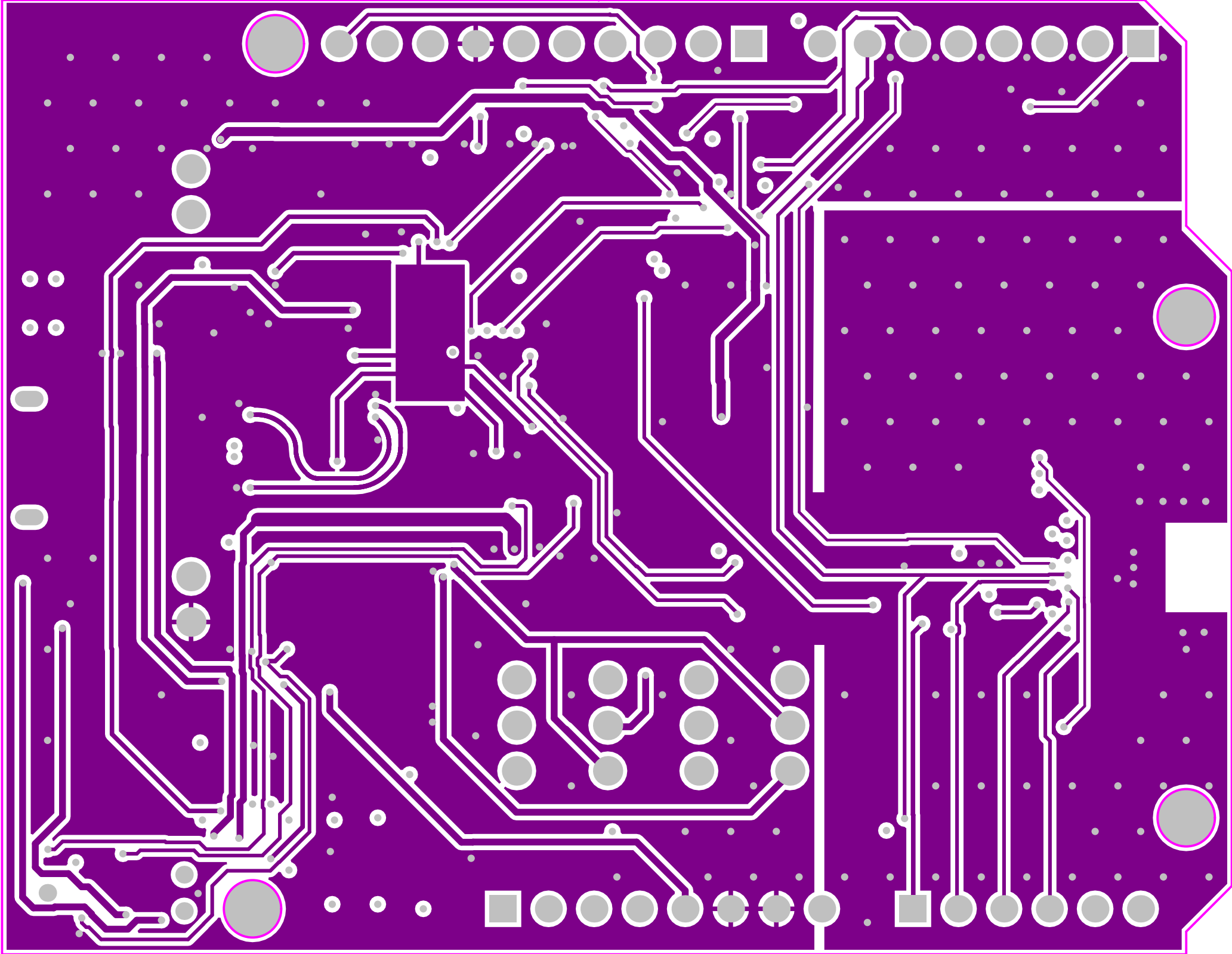
| | | | | | | | | | |
|-------------|---------|--------------------------------------|--|------------|------|------------------|---------------------------------|--------------|--|
| | | UNLESS OTHERWISE SPECIFIED: | | NAME | DATE | ON Semiconductor | | | |
| | | DIMENSIONS ARE IN INCHES | | DRAWN | M.C. | 6/13/2018 | TITLE RSL10 SiP EVB V1.2 | | |
| | | TOLERANCES: | | CHECKED | | | | | |
| | | FRACTIONAL ± | | ENG APPR. | | | | | |
| | | ANGULAR: MACH± BEND ± | | MFG APPR. | | | | | |
| | | TWO PLACE DECIMAL ± | | Q.A. | | | | | |
| | | THREE PLACE DECIMAL ± | | COMMENTS: | | | | | |
| | | INTERPRET GEOMETRIC TOLERANCING PER: | | | | | SIZE | DWG. NO. | |
| | | MATERIAL | | | | | | | |
| NEXT ASSY | USED ON | FINISH | | | | | | | |
| APPLICATION | | DO NOT SCALE DRAWING | | | | | | | |
| | | | | SCALE: 1:1 | | WEIGHT: | | SHEET 1 OF 1 | |

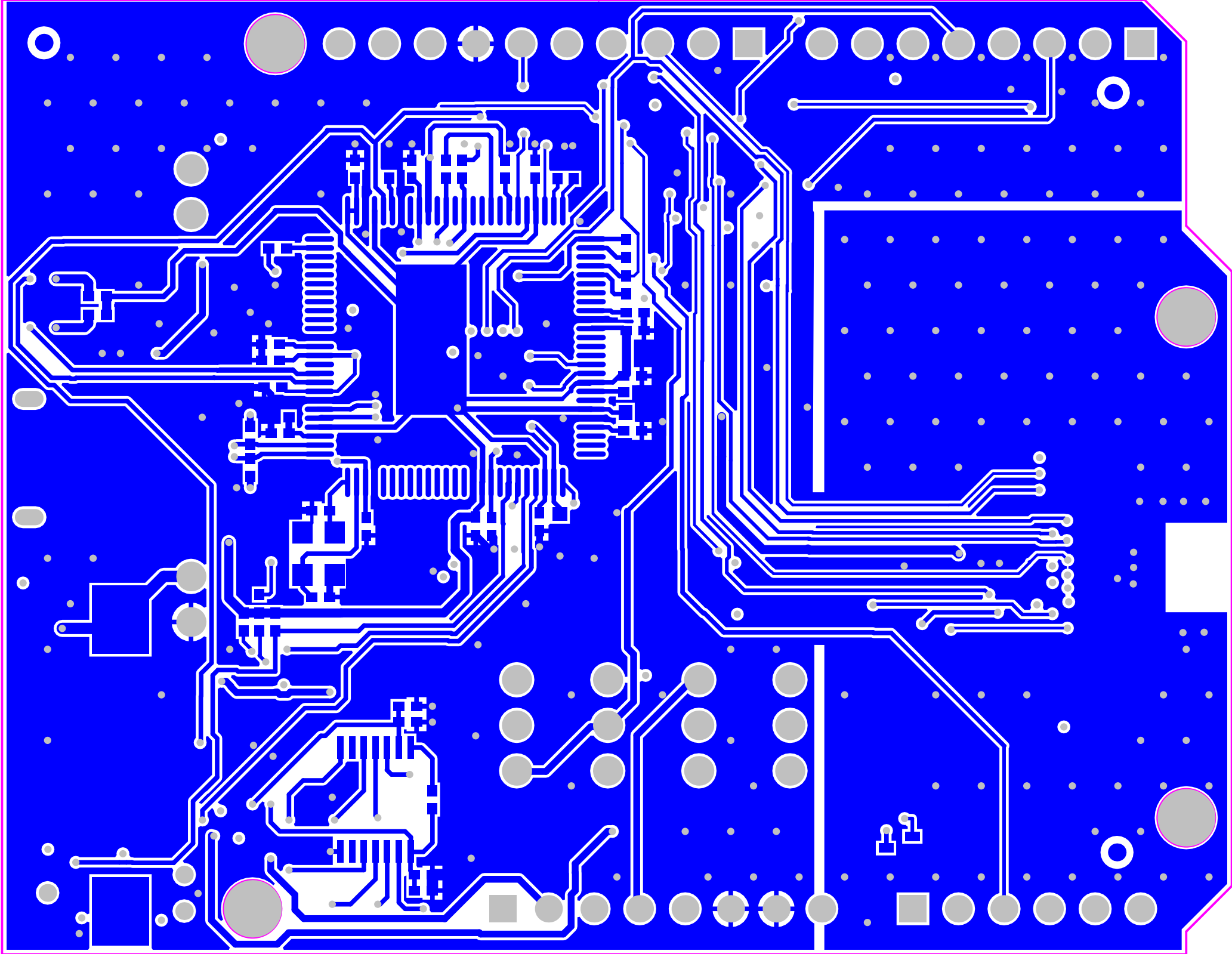


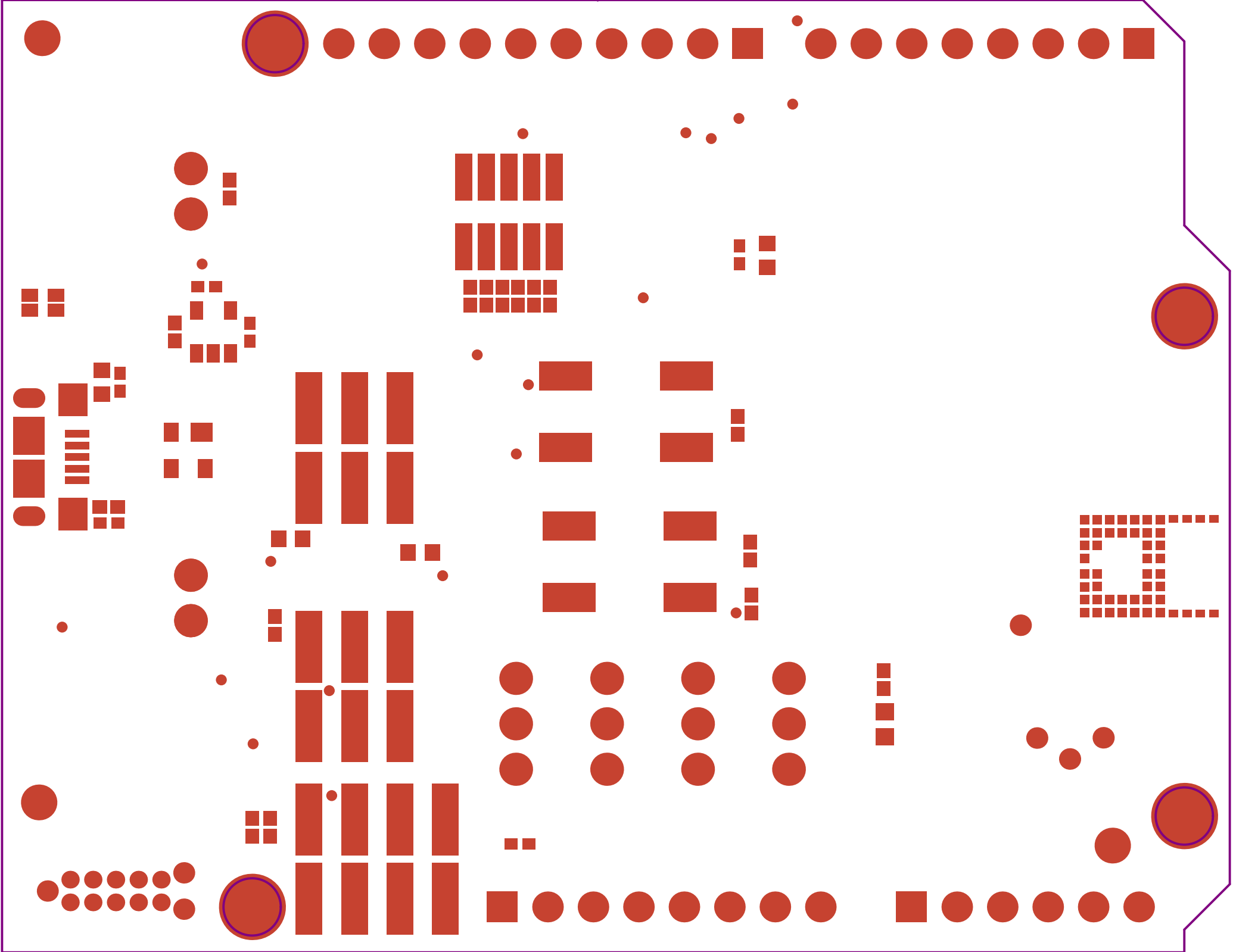


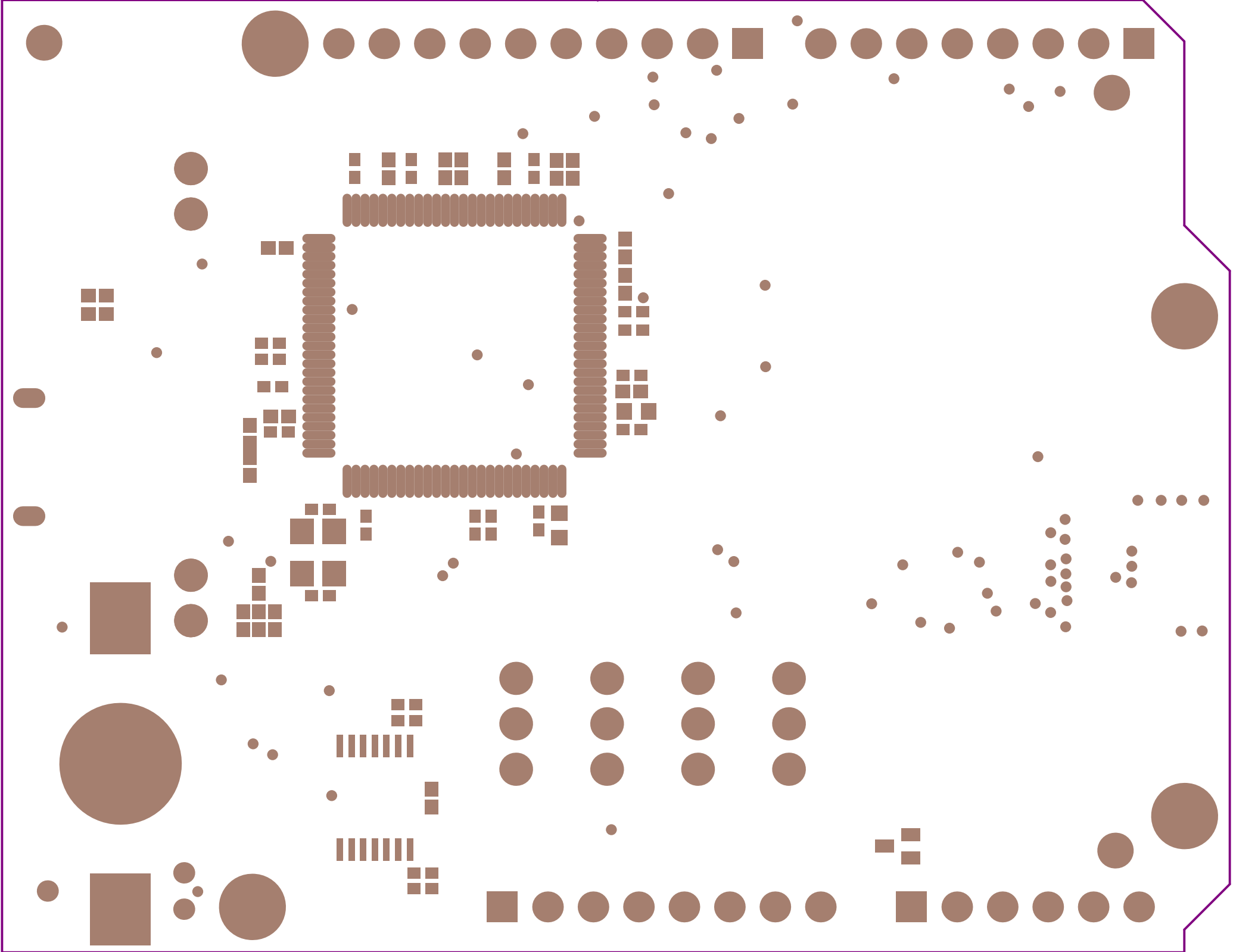


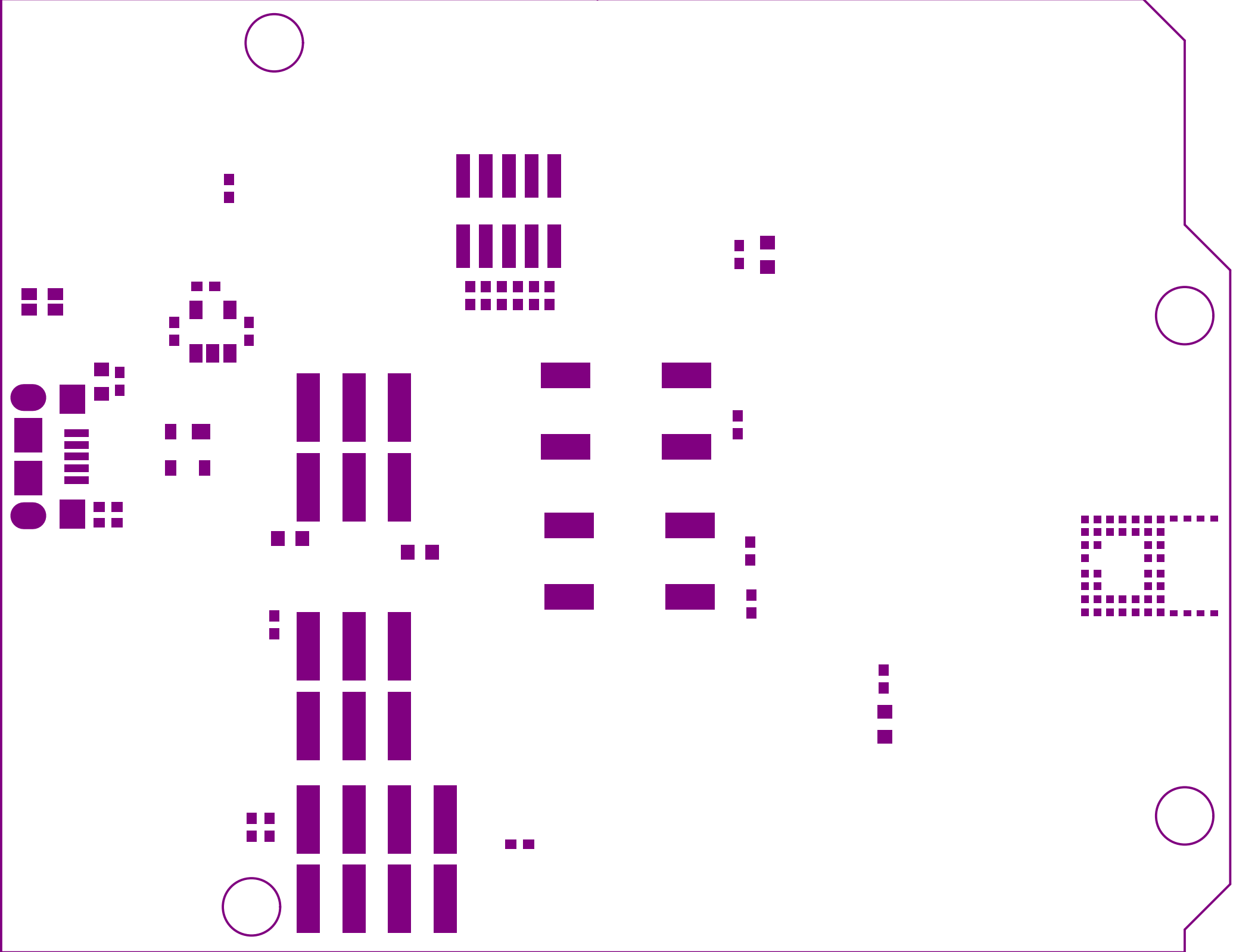


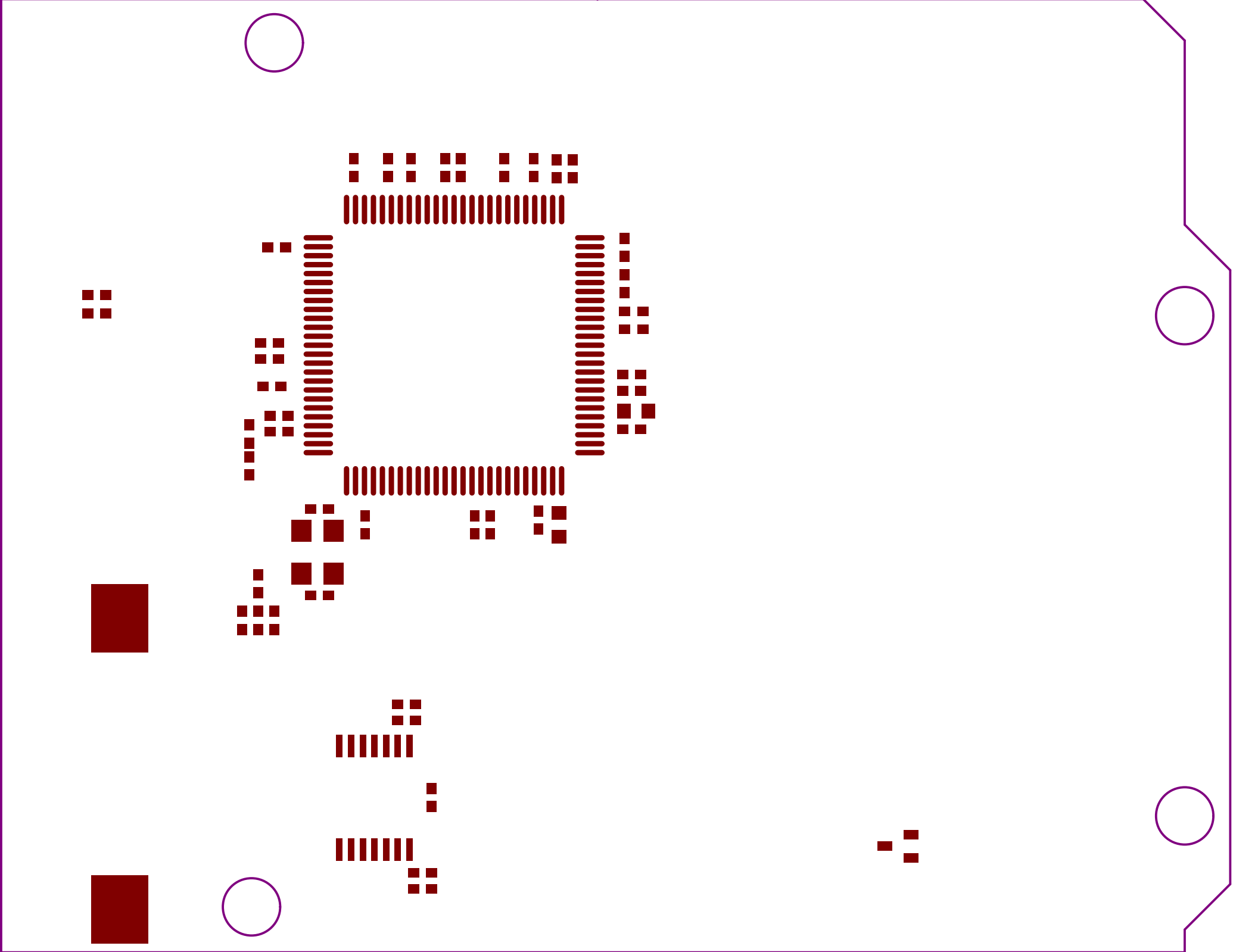


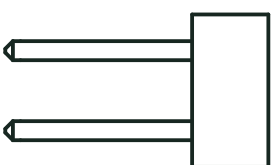
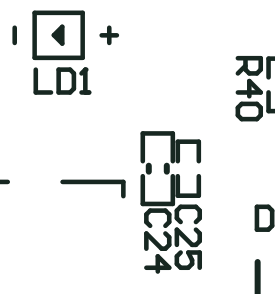
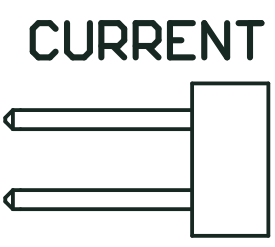




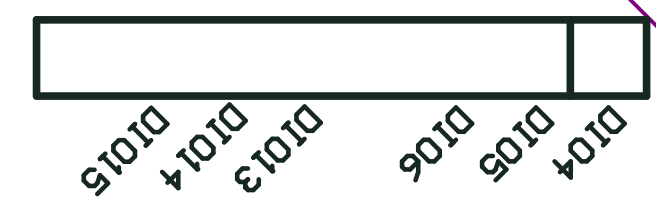
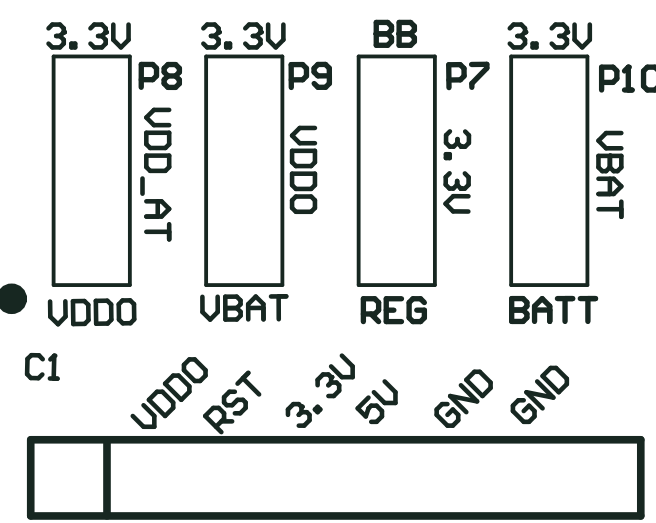
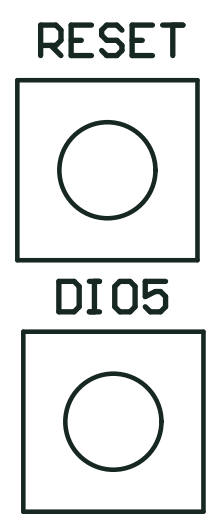
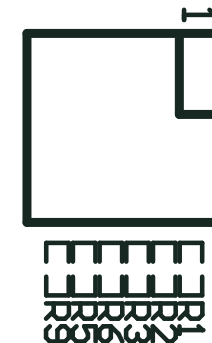
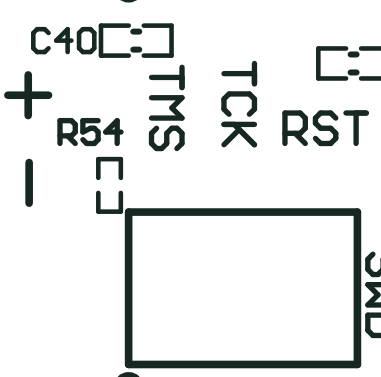
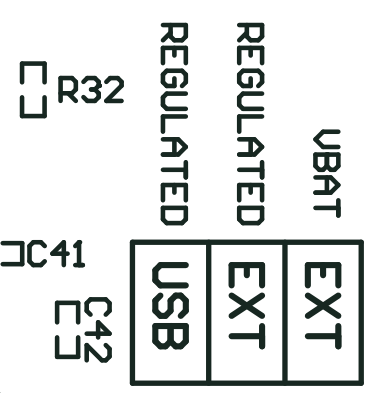




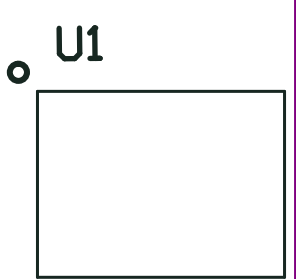
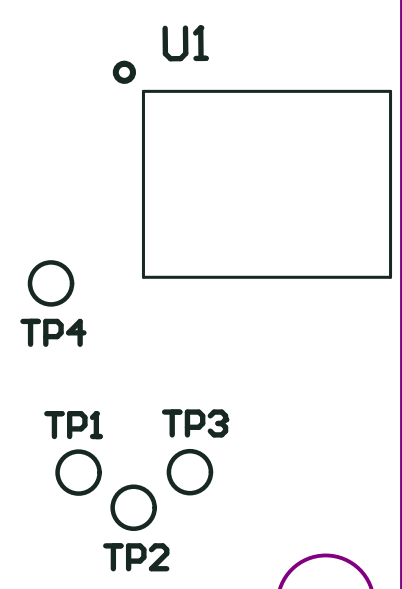
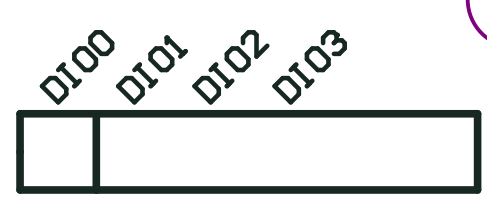
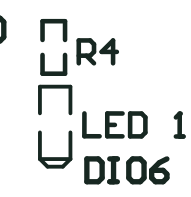




JTAG MCU



RSL10 SiP
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RSL10 SiP EVB V1.2
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May 2018

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